Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A method comprising:

receiving a packet in a packet processor, the packet processor comprising:

a stack processor

a hardware scheduler in the stack processor;

a control processor; and

a packet engine managed by the control processor;

scheduling processing of [[a]] the packet received by [[a]] the packet processor with [[a]] the hardware scheduler ~~in a stack processor included in the packet processor~~, wherein scheduling includes receiving an interrupt signal from the packet engine.

2. (Cancelled)

3. (Original) The method of claim 1 wherein the scheduling includes identifying an interrupt handling routine.

4. (Cancelled)

5. (Original) The method of claim 1 wherein the scheduler uses a weighted round robin scheduling scheme.

6. (Original) The method of claim 1 wherein the stack processor receives the packet for a scratch ring included in the packet processor.

7. (Currently Amended) The method of claim [[4]] 1 wherein the stack processor passes a message through a communication queue to the control processor.

8. (Currently Amended) A computer program product, tangibly embodied in ~~an information carrier~~ a computer-readable storage medium, the computer program product being operable to cause a machine to:

schedule processing of a packet received by a packet processor with a hardware scheduler ~~in a stack processor included in the packet processor~~, wherein scheduling includes receiving an interrupt signal from the packet engine.

9. (Cancelled)

10. (Original) The computer program product of claim 8 wherein the instructions to schedule include instructions to identify an interrupt handling routine.

11. (Cancelled)

12. (Original) The computer program product of claim 8 wherein instructions to schedule use a weighted round robin scheduling scheme.

13. (Original) The computer program product of claim 8 wherein the stack processor receives the packet from a scratch ring included in the packet processor.

14. (Currently Amended) The computer program product of claim [[11]] 8 wherein the stack processor passes a message through a communication queue to the control processor.

15. (Currently Amended) A hardware scheduler comprises:

~~a process~~ a processor configured to schedule processing of a packet received by [[a]] the packet processor ~~with a hardware scheduler in a stack processor included in the packet processor,~~ wherein scheduling includes receiving an interrupt signal from a packet engine managed by a control processor included in the packet processor.

16. (Cancelled)

17. (Original) The scheduler of claim 15 wherein the scheduling includes identifying an interrupt handling routine.

18. (Currently Amended) A system comprising:

a packet processor capable of,

scheduling processing of a packet received by the packet processor with a hardware scheduler in a stack processor included in the packet processor; wherein scheduling includes receiving an interrupt signal from a packet engine managed by a control processor included in the packet processor.

19. (Cancelled)

20. (Original) The system of claim 18 wherein scheduling includes identifying an interrupt handling routine.

21. (Currently Amended) A packet forwarding device comprising:

an input port for receiving packets;

an output for delivering the received packets; and

a packet processor capable of,

scheduling processing of a packet received by the packet processor with a hardware scheduler in a stack processor included in the packet processor; wherein scheduling includes

receiving an interrupt signal from a packet engine managed by a control processor included in the packet processor.

22. (Cancelled)

23. (Original) The packet forwarding device of claim 21 wherein scheduling includes identifying an interrupt handling routine.

24. (Currently Amended) A packet processor comprising:

a packet engine for receiving a packet;

a control processor for managing the packet engine; and

a stack processor for scheduling processing of the received packet with a hardware scheduler;

wherein scheduling includes receiving an interrupt signal from the packet engine.

25. (Cancelled)

26. (Original) The packet processor of claim 24 wherein the hardware scheduler identifies an interrupt handling routine.